BOOST CIRCUIT

Wayne M. Struble

Related Applications

[0001] This application relates to and claims priority of U.S. Provisional Application Serial No.: 60/471,109 filed May 16, 2003.

FIELD OF THE INVENTION

[0002] The present invention relates to a circuit for boosting a DC voltage using a radio frequency (RF) input signal, wherein the boost circuit does not significantly load (attenuate) the RF signal path.

RELATED ART

[0003] Fig. 1 is a circuit diagram of a conventional art single pole, four throw (SP4T) high-power field effect transistor (FET) RF switch 100. RF switch 100 includes resistors 110-113, 120-123, 130-133, 140-143 and 150-154, capacitors 160-164, RF sources 171-174 and n-channel field effect transistors 114-116, 124-126, 134-136 and 144-146, which are connected as illustrated. Resistors 110-113 and transistors 114-116 form a first switch element 191; resistors 120-123 and transistors 124-126 form a second switch element 192; resistors 130-133 and transistors 134-136 form a third switch element 193; and resistors 140-143 and transistors 144-146 form a fourth switch element 194.

[0004] During normal operation, one (or none) of the switch elements 191-194 is enabled. To enable one of the switch elements 191-194, a corresponding DC control voltage V_{C1}-V_{C4} is activated, thereby turning on an associated set of switch transistors 114-116, 124-126, 134-125 or 144-146. For example, switch element 191 may be enabled by activating

DC control voltage V_{C1}. The activated control voltage V_{C1} turns on transistors 114-116 (via resistors 110-113), thereby allowing an RF signal from RF source 171 to be routed through input resistor 151, input capacitor 161, transistors 114-116 and output capacitor 160 to load resistor 150. The input resistor 151 and load resistor 150 are typically matched. For example, input resistor 151 and load resistor 150 may each have a resistance of 50 Ohms. In this example, the DC control voltages V_{C2}-V_{C4} are deactivated, such that switch elements 191-194 are disabled.

[0005] The activated control voltage (e.g., V_{C1}) is typically provided by (or derived from) a system voltage supply. For example, the activated control voltage V_{C1} may have a nominal value of about 2.5 Volts. When the control voltage V_{C1} Is activated, a small DC control current I_{C1} flows through resistor 110 (to resistors 111-113).

[0006] It is desirable for RF switch 100 to operate in a linear manner, with a low control current (e.g., I_{C1}). However, semiconductor switches, such as RF switch 100, are inherently non-linear. Output harmonics, which add distortion to the RF output signal, are generated as a result of the non-linear behavior of the semiconductor RF switch 100. These output harmonics increase significantly as the control voltage (e.g., V_{C1}) decreases. For example, the harmonics may increase significantly if the control voltage V_{C1} drops below 2.5 Volts.

[0007] It would therefore be desirable to have an RF switch that is capable of operating in a highly linear manner in response to a low control voltage. It would further be desirable if such an RF switch did not consume excessive layout area on a semiconductor chip. It would further be desirable if such an RF switch did not add

significant non-linearity to the RF signal path. It would further be desirable if such an RF switch did not significantly increase the required DC control current. It would further be desirable if such an RF switch did not exhibit a substantially higher insertion loss than RF switch 100.

SUMMARY OF THE INVENTION

[0008] Accordingly, the present invention provides a DC voltage boost circuit that provides a boosted DC output voltage in response to an RF input signal. The boosted DC output voltage can be a negative or positive voltage, depending on the configuration of the DC voltage boost circuit. The DC voltage boost circuit includes a capacitor coupled to receive the RF input signal, a high impedance rectifier circuit coupled to the capacitor, and a bias extractor circuit (which provides the boosted DC output voltage) coupled to the high impedance rectifier circuit.

[0009] The high impedance rectifier circuit advantageously prevents a high current from being drawn from the source of the RF input signal. As a result, the DC voltage boost circuit adds only a minimal insertion loss to the RF input signal.

[0010] In one embodiment, a DC control voltage is applied to the rectifier circuit, whereby the DC voltage boost circuit effectively boosts the DC control voltage to create the boosted DC output voltage. In one embodiment, the boosted DC output voltage is equal to the DC control voltage, plus about 2 Volts.

[0011] The boosted DC output voltage can be used, for example, to control an RF switch element. In this embodiment, the RF input signal is routed through the RF

switch element. The relatively high boosted DC output voltage is used to turn on the RF switch element, thereby minimizing output harmonics in the RF output signal routed from the RF switch element.

[0012] The present invention will be more fully understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Fig. 1 is a circuit diagram of a conventional SP4T high-power FET RF switch.

[0014] Fig. 2 is a circuit diagram of a SP4T high-power FET RF switch that includes four boost circuits in accordance with one embodiment of the present invention.

[0015] Fig. 3 is a block diagram that illustrates a portion of the RF switch of Fig. 2 in accordance with one embodiment of the present invention.

[0016] Fig. 4 is a circuit diagram of DC boost circuit in accordance with one embodiment of the present invention.

[0017] Fig. 5 is a graph that illustrates the DC voltage (V_G) applied to the gates of transistors in an RF switch without a DC boost circuit, and the DC voltage (V_G) applied to the gates of transistors in RF switch with a DC boost circuit, with respect to a DC control voltage V_{C1}.

[0018] Fig. 6 is a graph that illustrates the DC control current (I_{C1}) drawn from the DC voltage supply in an RF switch without a boost circuit and an RF switch with a boost circuit, with respect to a DC control voltage V_{C1}.

[0019] Fig. 7 is a graph that illustrates the second and third output harmonics for an RF switch without a boost circuit and an RF switch with a boost circuit, with respect to a control voltage V_{C1}.

[0020] Fig. 8 is a graph that compares the insertion loss of an RF switch without a boost circuit and an RF switch with a boost circuit, with respect to frequency of an RF input signal R_{FIN1}.

[0021] Fig. 9 is a layout diagram illustrating the DC boost circuit of Fig. 4 in accordance with one embodiment of the present invention.

[0022] Figs. 10-22 are circuit diagrams illustrating variations of the DC boost circuit of Fig. 4, in accordance with different embodiments of the present invention.

DETAILED DESCRIPTION

[0023] Fig. 2 is a circuit diagram of a single pole, four throw (SP4T) high-power FET RF switch 200, which includes boost circuits 201-204 in accordance with one embodiment of the present invention. Although the present embodiment includes boost circuits used in connection with a SP4T switch, one of ordinary skill in the art would understand how to use the boost circuit of the present invention in other switch configurations. Because RF switch 200 is similar to RF switch 100 (Fig. 1), similar elements in Figs. 1 and 2 are labeled with similar reference numbers. In addition to resistors 110-113, 120-123, 130-133, 140-143 and 150-154, n-channel FETs 114-116, 124-126, 134-136 and 144-146, capacitors 160-164, RF sources 171-174, RF switch 200 includes DC boost circuits 201-204. Because DC boost circuits 201-204 modify the operation of switch elements 191-194, these switch elements are relabeled as switch elements 211-214 in Fig. 2.

[0024] Each of DC boost circuits 201-204 is configured to receive a corresponding DC control voltage V_{C1}-V_{C4}, respectively, and a corresponding RF input signal RF_{IN1}-RF_{IN4},

respectively. In response, each of DC boost circuits 201-204 provides a boosted DC output voltage DC_{OUT1}-DC_{OUT4}, respectively. These boosted DC output voltages DC_{OUT1}-DC_{OUT4}, are provided to the gates of switch transistors 114-116, 124-126, 134-136 and 144-146, respectively. Although three switch transistors (and three associated resistors) are present in each of switch elements 211-214 in the described embodiment, it is understood that other numbers of switch transistors (and associated resistors) can be used in other embodiments. Moreover, although the boosted DC output voltages DC_{OUT1}-DC_{OUT4} are used to drive switch elements 211-214, respectively, in the described embodiment, it is understood that such DC boost circuits 201-204 can also be used to generate DC output voltages DC_{OUT1}-DC_{OUT4} for other purposes in other applications.

[0025] At most, one of the switch elements 211-214 is activated at any given time. Consequently, the present embodiment will be described in more detail with respect to switch element 211 and the associated DC boost circuit 201. However, it is understood that switch elements 212-214 and the associated DC boost circuits 202-204 operate in the same manner.

[0026] Fig. 3 is a block diagram that illustrates resistors 150-151, RF source 171, DC boost circuit 201 and switch element 211. Capacitors 160-161 are not shown in Fig. 3 for purposes of clarity. DC boost circuit 201 is coupled in a shunt configuration with a radio frequency signal path comprising RF input signal source 171 and resistors 150-151. As described in more detail below, DC boost circuit 201 can be used to boost the voltage associated with an existing DC voltage source (which provides DC control voltage V_{C1}) to a higher (or lower)

value, without significantly increasing the current (I_{C1}) supplied by the DC voltage source.

[0027] Fig. 4 is a circuit diagram of DC boost circuit 201 in accordance with one embodiment of the present invention. DC boost circuit 201 includes capacitors 401-402, diode elements 411-412 and resistors 421-423, which are connected as illustrated. Diode elements 411-412 and resistors 421-422 are configured to form a rectifier circuit 431. Capacitor 402 and resistor 423 are configured to form a bias extractor circuit 432. In general, DC boost circuit 201 operates as follows in response to a positive DC input voltage V_{C1}. The RF_{IN1} signal oscillates between negative voltages and positive voltages. When the RF_{IN1} signal has a sufficiently low/negative voltage, diode element 411 turns on and capacitor 401 charges in the direction illustrated by dashed line 450. At this time, diode element 412 is turned off, and the DC_{OUT1} voltage is supplied by capacitor 402, as illustrated by dashed line 451.

[0028] When the RF_{IN1} signal has a sufficiently high/positive voltage, diode element 412 turns on, and capacitor 401 discharges to provide the DC_{OUT1} voltage, in the direction illustrated by dashed line 452. At this time, diode element 411 is turned off, and capacitor 402 charges in the direction illustrated by dashed line 453.

[0029] As described above, diode elements 411 and 412 operate as a rectifier circuit. Resistors 421 and 422 present a high impedance to RF source 171 (i.e., provide a high input impedance for the rectifier circuit). As a result, resistors 421 and 422 advantageously prevent DC boost circuit 201 from drawing a high current from RF source 171. Capacitor 402 (and resistor 423) operate as a bias extractor, which provides the boosted DC output voltage DC_{OUT1}

to switch element 191 in response to the charge pumped through the rectifier circuit. DC boost circuit 201 advantageously provides a high AC impedance at the DC_{OUT1} output terminal.

[0030] As described in more detail below, boost circuit 201 is used to overcome the deleterious effect of a low DC control voltage (e.g., VC_1) on the harmonic performance of a high-power FET RF switch. To accomplish this, boost circuit 201 uses a portion of the RF input signal (e.g., R_{FIN1}) to increase the effective switch control voltage. (e.g., the voltage on the gates of switch transistors 114-116).

[0031] In the forgoing manner, DC boost circuit 201 provides the DC_{OUT1} voltage in response to the RF_{IN1} signal and the V_{C1} control voltage. In a particular embodiment, capacitor 401 has a capacitance of 0.4 picoFarads (pF) and capacitor 402 has a capacitance of 0.8 pF. In this embodiment, each of diode elements 411 and 412 are made of an n-channel field effect transistor having commonly coupled source and drain regions. The channel region of each transistor has a width of about 10 microns. The gate of the transistor forms the anode of the diode element, and the commonly coupled source and drain regions form the cathode of the diode element. Although each of diode elements 411 and 412 is made of a single diode in the described embodiment, it is understood that in other embodiments, each of diode elements 411 and 412 can be made of a plurality of diodes. These diodes can be connected, for example, in series. Resistors 421 and 422 each have a resistance of about 15 kilo-Ohms (kΩ), and resistor 423 has a resistance of about 10 kΩ. In this embodiment, boost circuit 201 can

easily generate 5-6 Volts of DC voltage boost (positive or negative) from a 1-2 Watt RF input signal, RF_{IN1}.

[0032] Fig. 5 is a graph 500 that illustrates the DC voltage (V_G) applied to the gates of transistors 114-116 in RF switch 100 (without a DC boost circuit), and the DC voltage (V_G) applied to the gates of transistors 114-116 in RF switch 200 (with DC boost circuit 201), with respect to the DC control voltage V_{C1}. This graph 500 assumes that the RF input signal RF_{IN1} has a frequency of 1 GHz and an input power of 34 dBm. The DC gate voltage V_G of RF switch 100 is illustrated as line 501, and the DC gate voltage V_G of RF switch 200 is illustrated as line 502. For RF switch 100, the DC gate voltage V_G applied to the gates of transistors 114-116 is always slightly less than the control voltage V_{C1}. However, for RF switch 200, the DC gate voltage V_G applied to the gates of transistors 114-116 is about 2 Volts greater than the control voltage V_{C1}. As described in more detail below, this high gate voltage V_G advantageously improves the linearity of RF switch 200 by minimizing output harmonics.

[0033] Fig. 6 is a graph 600 that illustrates the DC control current (I_{C1}) drawn from the DC voltage supply in RF switch 100 and RF switch 200, with respect to the DC control voltage V_{C1}. Like graph 500, graph 600 also assumes that the RF_{IN1} signal has a frequency of 1 GHz and an input power of 34 dBm. The DC control current I_{C1} drawn from the DC voltage supply in RF switch 100 is illustrated as line 601, and the DC control current I_{C1} drawn from the DC voltage supply in RF switch 200 is illustrated as line 602. At voltages greater than about 2.5 Volts, the DC control current I_{C1} drawn from the DC voltage supply in RF switch 200 is only slightly greater than the DC control current I_{C1} drawn from the DC voltage supply in RF switch 100. More specifically, the DC

control current I_{C1} drawn from the DC voltage supply in RF switch 200 is only about 5 to 6 micro-Amps (μA) greater than the DC control current I_{C1} drawn from the DC voltage supply in RF switch 100 for control voltages V_{C1} greater than 2.5 Volts. Advantageously, DC boost circuit 201 does not require an excessive amount of additional current from the DC voltage supply.

[0034] Fig. 7 is a graph 700 that illustrates the second and third output harmonics for RF switch 100 and RF switch 200, with respect to the control voltage V_{C1}. Like graphs 500 and 600, graph 700 also assumes that the RF_{IN1} signal has a frequency of 1 GHz and an input power of 34 dBm. The second and third output harmonics of RF switch 100 are illustrated as lines 701-702, respectively. The second and third output harmonics of RF switch 200 are illustrated as lines 711-712, respectively. The output harmonics are measured in decibels down from the carrier signal, or dBc. A higher dBc value represents smaller harmonics, and therefore a more linear transfer function within the RF switch. For a control voltage V_{C1} less than about 2.5 Volts, the third harmonics of RF circuit 100 are significantly lower than the third harmonics of RF circuit 200. Similarly, for a control voltage V_{C1} less than about 2 Volts, the second harmonics of RF circuit 100 are significantly lower than the second harmonics of RF circuit 200. Thus, for a control voltage V_{C1} less than about 2.5 Volts, RF switch 200 advantageously operates in a significantly more linear manner than RF switch 100.

[0035] Fig. 8 is a graph 800 that compares the insertion loss of RF switch 100 with the insertion loss of RF switch 200, with respect to frequency of the RF input signal R_{FIN1}.

In general, insertion loss is a measure of output power with respect to input power. The insertion loss of RF switch 100 is illustrated as line 801, and the insertion loss of RF switch 200 is illustrated as line 802. As illustrated, there is very little insertion loss associated with the addition of DC boost circuit 201. For example, at a frequency of 1 giga-Hertz (GHz), DC boost circuit 201 only adds about 0.05 dB of insertion loss (or about 8% insertion loss). In general, boost circuit 201 provides an RF signal path attenuation of only about 0.04-0.05 dB.

[0036] Fig. 9 is a layout diagram illustrating DC boost circuit 201 in accordance with one embodiment of the present invention. This layout diagram illustrates diode elements 411-412, which are diode-connected FETs (as described above); resistors 421-423, which can be epitaxial, bulk, high resistivity metal (e.g., nichrome, tungsten silicide, tungsten nitride) or polysilicon traces; and capacitors 401-402, which are formed by a semiconductor substrate, a first metal layer formed over the semiconductor substrate, a dielectric layer formed over the first metal layer, and a second metal layer (e.g., gold) formed over the dielectric layer. Advantageously, DC boost circuit 201 can be implemented using standard semiconductor fabrication techniques in a relatively small area. For example, DC boost circuit 201 can have an area of about 70 x 110 microns^2 using a conventional 0.5 micron gallium arsenide pseudomorphic high electron mobility transistor (PHEMT) process. Consequently, DC boost circuit 201 is ideal for low cost applications. Other acceptable processes for fabricating DC boost circuit 201 include a CMOS process, a silicon-on-insulator (SOI) process, or any ion implanted MESFET process.

[0037] DC boost circuit 201 can be modified in accordance with other embodiments of the present invention. Figs. 10-22 are circuit diagrams illustrating variations of DC boost circuit 201 in accordance with various embodiments of the present invention. Because the DC boost circuits of Figs. 10-22 are similar to DC boost circuit 201 (Fig. 4), similar elements in Figs. 4 and 10-22 are labeled with similar reference numbers.

[0038] Fig. 10 is a circuit diagram of DC boost circuit 1001, in accordance with one embodiment of the present invention. DC boost circuit 1001 is similar to DC boost circuit 201. However, capacitor 402 is coupled to receive the ground supply voltage, rather than the V_{C1} voltage. The connection of capacitor 402 to the ground voltage supply makes this configuration slightly more complex. This configuration results in rectifier circuit 1031 and bias extractor 1032.

[0039] Fig. 11 is a circuit diagram of DC boost circuit 1101, in accordance with another embodiment of the present invention. DC boost circuit 1101 is similar to DC boost circuit 1001. However, capacitor 402 is coupled to the output terminal of the DC boost circuit, rather than the ground voltage supply. This configuration results in bias extractor circuit 1132.

[0040] Fig. 12 is a circuit diagram of DC boost circuit 1201, in accordance with another embodiment of the present invention. DC boost circuit 1201 is similar to DC boost circuit 1001. However, capacitor 402 is eliminated from DC boost circuit 1201. In this embodiment, the capacitance of the load (e.g., the gate capacitances of transistors 114-116) is used to replace capacitor 402. This configuration results in bias extractor circuit 1232.

[0041] Fig. 13 is a circuit diagram of DC boost circuit 1301, in accordance with another embodiment of the present invention. DC boost circuit 1301 is similar to DC boost circuit 201. However, the anode of diode element 441 is coupled to receive the ground supply voltage, rather than the V_{C1} voltage. The connection of diode element 411 to the ground voltage supply makes this configuration slightly more complex. This configuration results in rectifier circuit 1331 and bias extractor 1332.

[0042] Fig. 14 is a circuit diagram of DC boost circuit 1401, which is coupled to switch element 211 in accordance with another embodiment of the present invention. DC boost circuit 1401 is similar to DC boost circuit 1301. However, capacitor 402 is coupled to receive the ground supply voltage, rather than the V_{C1} voltage. Thus, DC boost circuit 1401 implements rectifier circuit 1331 and bias extractor 1032. Advantageously, DC boost circuit 1401 does not require a DC control voltage V_{C1}. The DC control voltage V_{C1} is also eliminated from switch element 211 by coupling resistor 111 to ground, as illustrated. As a result, the control line associated with providing such a control voltage can be advantageously eliminated from an associated printed circuit board or module. DC boost circuit 1401 is especially useful in switches that operate at a relatively constant power, such as those used in wireless local area network (LAN) transmitters.

[0043] Fig. 15 is a circuit diagram of DC boost circuit 1501, in accordance with another embodiment of the present invention. DC boost circuit 1501 is similar to DC boost circuit 1401. However, capacitor 402 is eliminated from DC boost circuit 1501. In this embodiment, the capacitance of the load (e.g., the gate capacitances of transistors 114-

116) is used to replace capacitor 402. Advantageously, DC boost circuit 1501 does not require a DC control voltage V_{C1}.

[0044] Fig. 16 is a circuit diagram of DC boost circuit 1601, in accordance with one embodiment of the present invention. DC boost circuit 1601 is similar to DC boost circuit 201. However, the connections of diode elements 411 and 412 are reversed, thereby providing diode elements 1611 and 1612.

[0045] When the RF_{IN1} signal has a sufficiently low/negative voltage, diode element 1612 turns on and capacitor 401 charges in the direction illustrated by dashed line 1650. At this time, diode element 1611 is turned off, and the DC_{OUT1} voltage is supplied by capacitor 402.

[0046] When the RF_{IN1} signal has a sufficiently high/positive voltage, diode element 1611 turns on, and capacitor 401 discharges to the V_{C1} supply terminal, in the direction illustrated by dashed line 1651. At this time, diode element 1612 is turned off. This configuration ensures that the "boosted" output voltage DC_{OUT1} is less than the DC control voltage V_{C1}. Thus, if DC control voltage V_{C1} is a negative voltage, then DC_{OUT1} will be a more negative voltage (or "boosted" negative voltage). Thus, DC boost circuit 1601 may be referred to as a negative DC boost circuit.

[0047] Fig. 17 is a circuit diagram of DC boost circuit 1701, in accordance with one embodiment of the present invention. DC boost circuit 1701 is similar to DC boost circuit 1601. However, capacitor 402 is coupled to receive the ground supply voltage, rather than the V_{C1} voltage. The connection of capacitor 402 to the ground voltage supply makes this configuration slightly more complex. This

configuration results in rectifier circuit 1731 and bias extractor 1732.

[0048] Fig. 18 is a circuit diagram of DC boost circuit 1801, in accordance with another embodiment of the present invention. DC boost circuit 1801 is similar to DC boost circuit 1701. However, capacitor 402 is coupled to the output terminal of the DC boost circuit, rather than the ground voltage supply. This configuration results in bias extractor circuit 1832.

[0049] Fig. 19 is a circuit diagram of DC boost circuit 1901, in accordance with another embodiment of the present invention. DC boost circuit 1901 is similar to DC boost circuit 1601. However, capacitor 402 is eliminated from DC boost circuit 1901. In this embodiment, the capacitance of the load (e.g., the gate capacitances of transistors 114-116) is used to replace capacitor 402. This configuration results in bias extractor circuit 1932.

[0050] Fig. 20 is a circuit diagram of DC boost circuit 2001, in accordance with another embodiment of the present invention. DC boost circuit 2001 is similar to DC boost circuit 1601. However, the anode of diode element 1611 is coupled to receive the ground supply voltage, rather than the V_{C1} voltage. The connection of diode element 1611 to the ground voltage supply makes this configuration slightly more complex. This configuration results in rectifier circuit 2031 and bias extractor 2032.

[0051] Fig. 21 is a circuit diagram of DC boost circuit 2101, in accordance with another embodiment of the present invention. DC boost circuit 2101 is similar to DC boost circuit 2001. However, capacitor 402 is coupled to receive the ground supply voltage, rather than the V_{C1} voltage. Thus, DC boost circuit 2101 implements rectifier circuit

2031 and bias extractor 1732. Advantageously, DC boost circuit 1401 does not require a DC control voltage V_{C1}. DC boost circuit 2101 can be coupled to switch element 211 in the same manner as DC boost circuit 1401 (Fig. 14).

[0052] Fig. 22 is a circuit diagram of DC boost circuit 2201, in accordance with another embodiment of the present invention. DC boost circuit 2201 is similar to DC boost circuit 2101. However, capacitor 402 is eliminated is eliminated from DC boost circuit 2201. In this embodiment, the capacitance of the load (e.g., the gate capacitances of transistors 114-116) is used to replace capacitor 402. Advantageously, DC boost circuit 2201 does not require a DC control voltage V_{C1}.

[0053] The present invention includes a bias circuit comprising: a rectifier having a rectifier input, a DC control voltage input and a rectifier output, wherein the rectifier is configured to produce the rectifier output, while providing a substantially high input impedance at the rectifier input, a rectified voltage from an alternating input signal applied at the rectifier input; and a bias extractor having an extractor input, a control voltage input and an extractor output, coupled to the rectifier output, and being configured to produce at the extractor output a DC voltage that is greater in magnitude than the DC control voltage input.

[0054] Although the invention has been described in connection with several embodiments, it is understood that this invention is not limited to the embodiments disclosed, but is capable of various modifications, which would be apparent to one of ordinary skill in the art.